Intel's 90 nm Logic Technology Using Strained Silicon Transistors

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90 nm Strained Silicon Transistors

- As first announced in 2002, Intel is employing a unique strained silicon transistor technology on its 90 nm logic process
- Intel is presenting a paper at the International Electron Devices Meeting in Washington, D.C. on December 9, 2003 that describes more details including the unique structure of our strained silicon transistors:

"A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors"

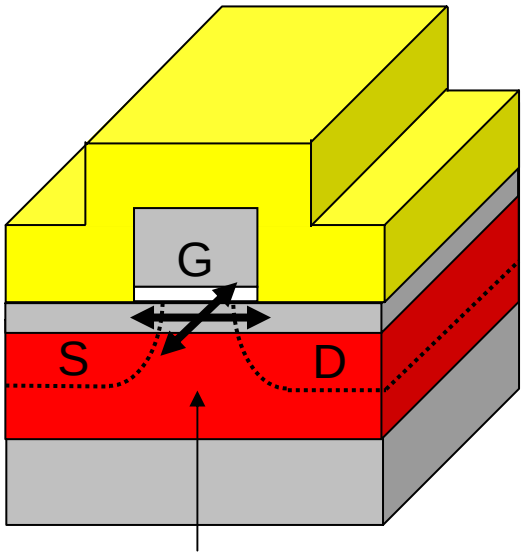
T. Ghani, et. al.

Portland Technology Development

Intel Corporation

Transistor Strain Techniques

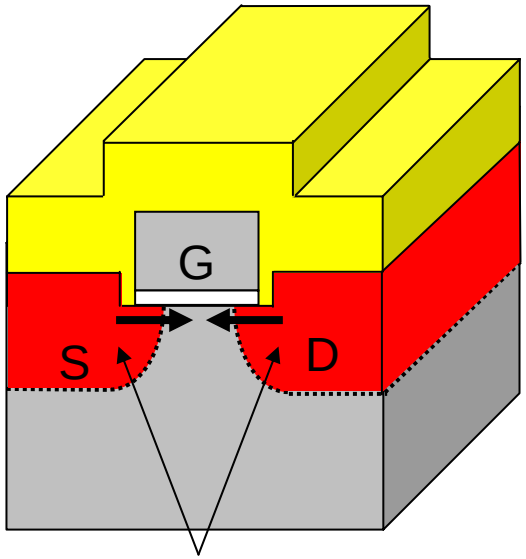
Traditional Approach



Graded SiGe Layer

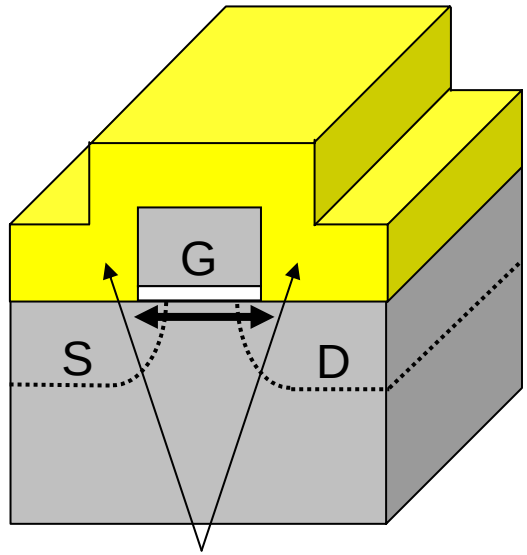
Biaxial
Tensile Strain

Intel's 90nm Technology



Selective SiGe S-D

Uniaxial
Compressive Strain
for PMOS



Tensile Si_3N_4 Cap

Uniaxial
Tensile Strain
for NMOS

Intel's Strained Silicon Transistors

- A unique selectively deposited SiGe source-drain structure induces channel strain in PMOS devices, improving drive current by 25% relative to non-strained devices
- A high stress Si_3N_4 cap layer induces channel strain in NMOS devices, improving drive current by 10% relative to non-strained devices
- NMOS and PMOS transistors are optimized separately for high performance using this approach to strain engineering and the added process cost is only ~2%
- This approach to transistor strain engineering is scalable to future generations

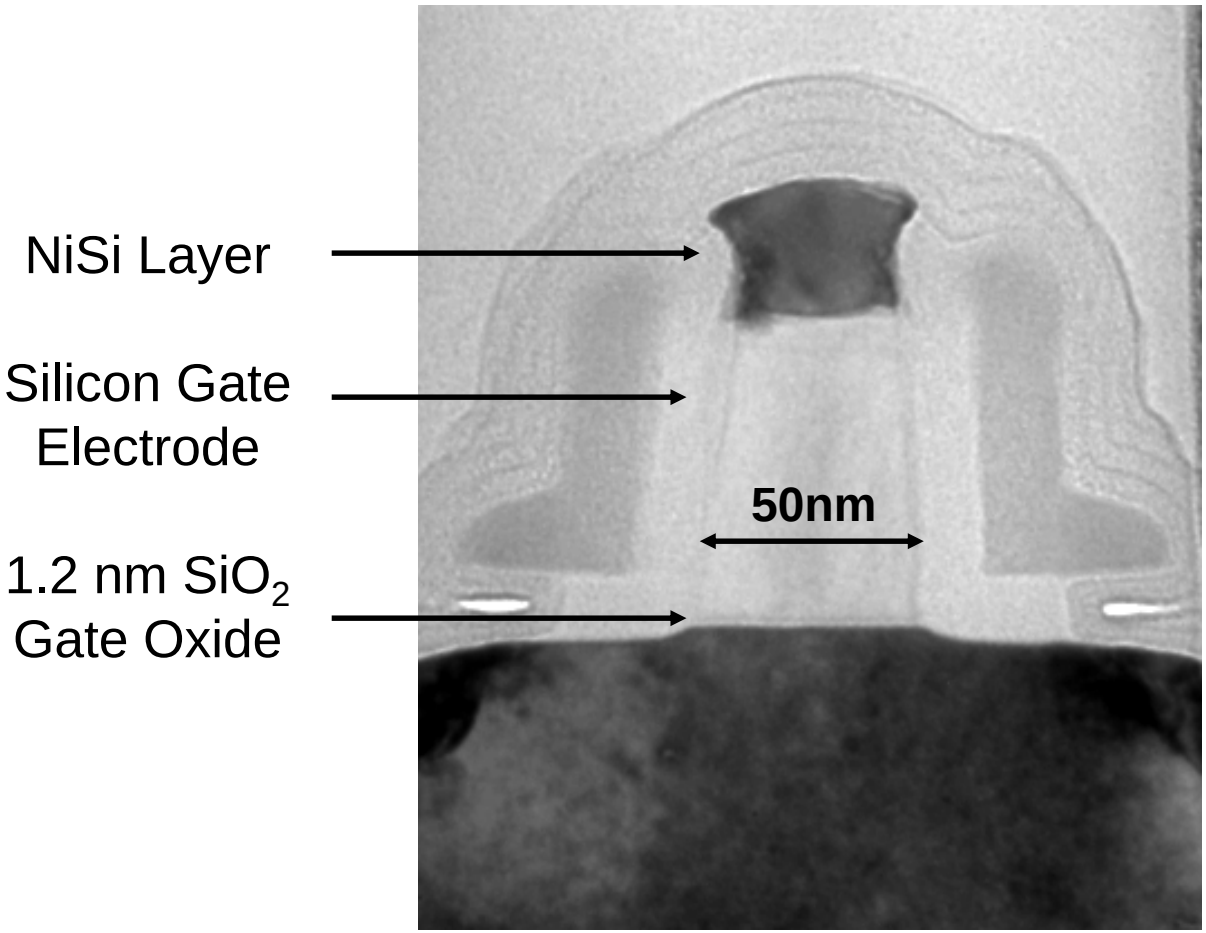
Intel's 90 nm Process Features

Other features of Intel's 90 nm logic technology include:

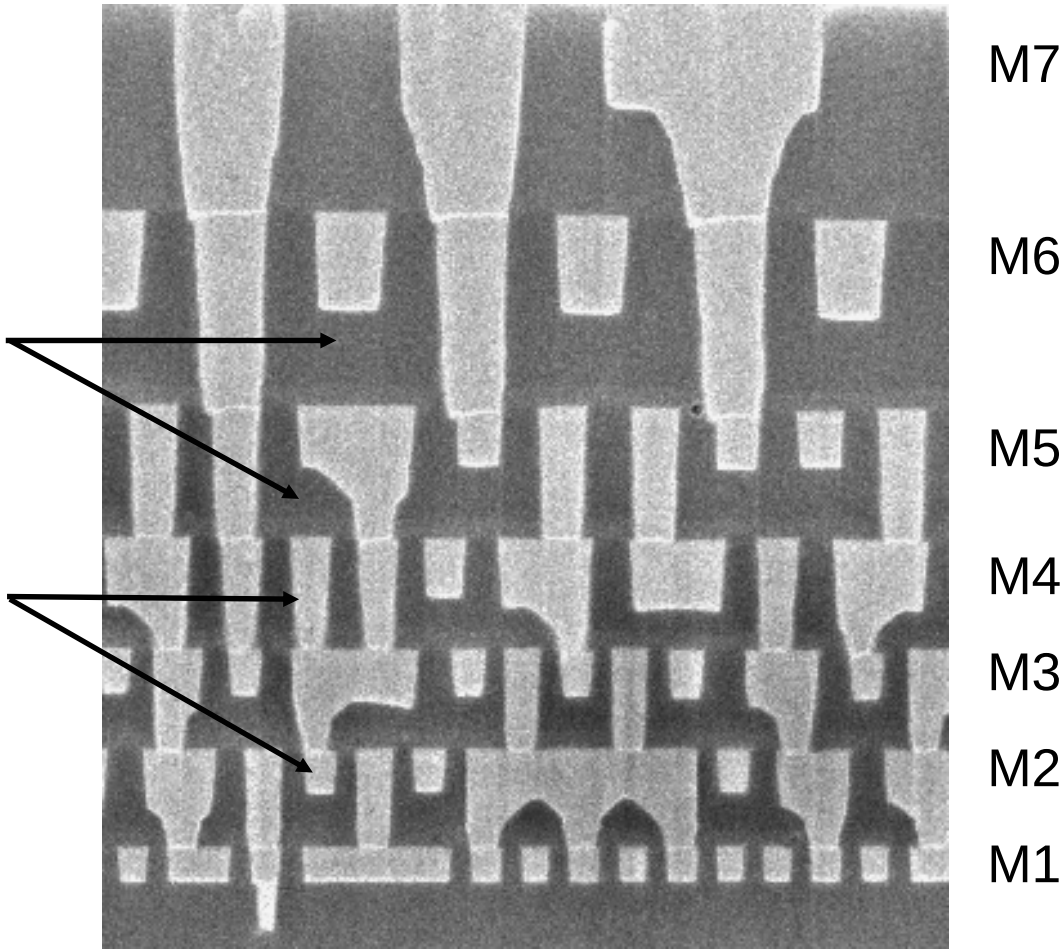
- 1.2 nm physical gate oxide thickness
- Nickel silicide
- 7 layers of copper interconnect
- Carbon doped oxide low-k dielectric
- 1.0 μm^2 6-T SRAM cell
- 300 mm wafers

Reference: S. Thompson, et. al., 2002 IEDM, p. 61

90 nm Generation Transistors



90 nm Generation Interconnects



1.0 μm^2 6-T SRAM Cell

90 nm Manufacturing Ramp

- Intel's 90 nm logic technology is presently being ramped to high volume on Pentium® and Centrino™ microprocessor products
- 300 mm fabs in Hillsboro, OR (D1C) and Albuquerque, NM (F11X) are ramping the 90 nm process in 2003, with a third fab in Leixlip, Ireland (F24) coming up in 1H 2004
- The 90 nm process has experienced rapid yield improvement and the defect density is now down to the low level needed for high volume manufacturing

Yield Trend for Intel Logic Technologies